

In re Application of WILLMAN  
Serial No. 10/208,975

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#### REMARKS

The Office action has been carefully considered. Claims 1-77 were rejected under 35 U.S.C. § 112, second paragraph, for being indefinite for failing to point out and distinctly claim the subject matter which the applicant regards as the invention. Claims 1-5, 7-34, and 36-77 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Magee et al., U.S. Patent No. 5,729,710 (hereinafter "Magee") in view of Williams U.S. Patent No. 6,304,973 (hereinafter "Williams"). Claims 6-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Magee in view of Williams, and in further view of Gulsen U.S. Patent No. 5,727,211 (hereinafter "Gulsen").

By present amendment, the Abstract has been amended. Applicant submits that the claims 1-77 as initially presented were in acceptable form. Independent claim 70 and dependent claims 74 and 75 have been amended to more particularly point out and distinctly claim the invention. Applicant further submits that the claims as filed were patentable over the prior art of record, and that the amendments herein are for purposes of clarifying the claims and/or for expediting allowance of the claims, and not for reasons related to patentability. Reconsideration is respectfully requested.

Applicant thanks the Examiner for the interview held (by telephone) on January 27, 2005. During the interview, the Examiner and applicants' attorney discussed the various sections of the application and independent claims 1, 32, 64, and 70 with respect to the prior art and enablement. The essence of applicant's position is incorporated in the remarks below.

Turning to the 35 U.S.C. § 112 rejections, the Office action has rejected independent claims 32 and 70 and dependent claims 74 and 75 for various antecedent basis

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issues, independent claims 1, 32, 64 and 70 and dependent claim 76 for indefiniteness, as well as dependent claims 31, 69, and 77 for limiting the method claims to computer-readable-medium claims. Applicant respectfully traverses these rejections.

Regarding the rejection of claims 31, 69, and 77 for limiting the method claims to computer-readable-medium claims, the Office action states, "... it is unclear whether the claims are independent or dependent claims. As is, computer-readable medium claims should not depend from computer-system claims." Office action, pg. 2, secs. 2b, 2g, and 2i. Applicant submits that the computer readable medium claims are structured to specifically associate the executable program instructions with the functions being performed, such that there is no doubt that the instructions performing these functions are stored on the computer readable medium. Regarding claim 31, claim 31 explicitly states a computer readable medium having the executable program instructions of claim 1. There is no doubt that executable program instructions of the steps recited in claim 1 are stored on the computer readable medium. MPEP § 2106(IV)(B)(1a). Reciting the steps in claim 31 merely places claim 1 in independent form and does not provide any greater clarity that the instruction performing the functions of the steps recited in claim 31 are stored on the computer readable medium. The rejection of claim 31 is respectfully traversed.

Regarding claim 69, claim 69 explicitly states a computer readable medium having the executable program instructions of claim 64. There is no doubt that executable program instructions of the steps recited in claim 64 are stored on the computer readable medium. MPEP § 2106(IV)(B)(1a). Reciting the steps in claim 69 merely places claim 64 in independent form and does not provide any greater clarity that the instruction performing

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the functions of the steps recited in claim 69 are stored on the computer readable medium.

The rejection of claim 69 is respectfully traversed.

Regarding claim 77, claim 77 explicitly states a computer readable medium having the executable program instructions of claim 70. There is no doubt that executable program instructions of the steps recited in claim 70 are stored on the computer readable medium. MPEP § 2106(IV)(B)(1a). Reciting the steps in claim 77 merely places claim 70 in independent form and does not provide any greater clarity that the instruction performing the functions of the steps recited in claim 77 are stored on the computer readable medium. The rejection of claim 77 is respectfully traversed.

Regarding the rejection of claim 1, the Office action states, "... 'a map' in line 5 is indefinite because it is not made explicitly clear in the claim language whether or not this is the same thing as 'a first memory map' (3-4)." Office action, pg. 2, sec. 2a. Applicant submits that the phrase "a map" is used in the claim language to modify the word "change" immediately following the phrase "a map" thereby resulting in the phrase "a map change." The context of the phrase "a map change" in claim 1 is that a privilege level is changed to allow "a map change" to occur. Hence, the phrase "a map" in line 5 of claim 1 is not indefinite. The rejection of claim 1 is respectfully traversed.

Regarding the rejection of claim 32 for indefiniteness, the Office action states, "... 'a protection mechanism' is indefinite because it is not made clear in the claim language what is being protected." Office action, pg. 2, sec. 2c. Applicant submits that lines 7 and 8 of claim 32 describe the "protection mechanism" as "configured to allow changing of a map." Furthermore, applicant's specification enables the "protection mechanism" at pg. 4, lines 13-17, pg. 5, lines 5-11, pg. 16, lines 2-9, and pg. 26 line 24 - pg. 27 line 6. The

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Federal Circuit has stated, "(i)t is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in a claim. See, e.g., *Loctite Corp. v. Ultra-seal Ltd.*, 781 F. 2d 861, 867, 228 U.S.P.Q. 90, 93 (Fed. Cir. 1985)." *Speciality Composites v. Cabot Corp.*, 845 F. 2d 981, 987 (Fed. Cir. 1988). Applicant submits that the "protection mechanism" is not indefinite as written in claim 32 and further that claim 32 is fully enabled in the specification. The rejection of claim 32 regarding indefiniteness is respectfully traversed.

Regarding the rejection of claim 32 for insufficient antecedent basis, the Office action states regarding, "... 'the thread' in lines 3 and 13. There is insufficient antecedent basis for this limitation in the claim. It is also unclear whether 'the thread' is only singular or could be plural by having at least one thread." Office action, pg. 2, sec. 2d. Applicant submits that by introducing "the thread" with the modifier of "at least one" that one or more threads are claimed in the system. Applicant further submits that the phrase "the thread" as used in lines 3 and 13 of claim 32 is proper usage of the phrase. The rejection of claim 32 regarding insufficient antecedent basis is respectfully traversed.

Regarding the rejection of claim 64 for indefiniteness, the Office action states, "... 'first and second address maps' is indefinite because it is not made explicitly clear in the claim language whether or not this is the same thing as a 'first and second memory map.'" Office action, pg. 2, sec. 2e. Applicant submits that the phrase 'first and second memory map' is not used in independent claim 64 nor in any claims that depend therefrom. Applicant further submits the phrase "first and second address maps" is fully enabled within applicant's specification at pg. 19, lines 10-13, pg. 19 line 21 – pg. 20 line 2, pg. 21, lines 12-19, pg. 25, lines 2-5, pg. 25 line 22 – pg. 26 line 14, and pg. 37, lines 1-5. The

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rejection of claim 64 regarding indefiniteness as to 'first and second memory map' is respectfully traversed.

Regarding the rejection of claim 64 for indefiniteness, the Office action states, "... 'changing the first address map to a second address map' (lines 20-21) is indefinite because it is unclear whether addresses or maps are being changed. In addition, it is unclear whether or not the first and address is a virtual address and physical address." Office action, pg. 3, sec. 2f. Applicant submits that a closer reading of claim 64 indicates that the "first address" portion of the "first address map" phrase describes the "map." Similarly, applicant submits that a closer reading of claim 64 indicates that the "second address" portion of the "second address map" phrase describes the "map." Applicant further submits the phrases "first address map" and "second address map" are fully enabled within applicant's specification at pg. 19, lines 10-13, pg. 19 line 21 – pg. 20 line 2, pg. 21, lines 12-19, pg. 25, lines 2-5, pg. 25 line 22 – pg. 26 line 14, and pg. 37, lines 1-5. Regarding the second portion of the rejection for indefiniteness, "[i]n addition, it is unclear whether or not the first and address is a virtual address and physical address" applicant is unclear as to what the Office action is referring to in claim 64. Applicant requests that the Examiner clarify the basis of the rejection. The rejection of claim 64 regarding indefiniteness as to 'changing the first address map to a second address map' and 'whether or not the first and address is a virtual address and physical address' is respectfully traversed.

Regarding the rejection of claim 70 for indefiniteness, the Office action states at sec. 2h, "... 'switching' and 'returning' is indefinite because it is not made explicitly clear in the claim language whether the map or the address is being switched and returned." Office action, pg. 3, sec. 2h. Applicant submits that a closer reading of claim 70 indicates that the

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"address" portion of the "address map" phrase describes the "map." Applicant further submits the phrase "address map" is fully enabled within applicant's specification at pg. 19, lines 10-13, pg. 19 line 21 - pg. 20 line 2, pg. 21, lines 12-19, pg. 25, lines 2-5, pg. 25 line 22 - pg. 26 line 14, and pg. 37, lines 1-5. Therefore, applicant submits that "switching" applies to "the second map" and that "returning" applies to "the first map." The rejection of claim 70 regarding indefiniteness as to "switching" and "returning" is respectfully traversed.

Regarding the rejection of claim 70 for indefiniteness at pg. 3, sec. 2i, as detailed above claim 70 has been amended to more particularly point out and distinctly claim the invention. The rejection of claim 70 as described at pg. 3, sec. 2i is respectfully traversed.

Regarding the rejection of claims 74 and 75 for insufficient antecedent basis at pg. 3, sec. 2j, as detailed above claims 74 and 75 have been amended to more particularly point out and distinctly claim the invention. The rejection of claims 74 and 75 as described at pg. 3, sec. 2i is respectfully traversed.

Regarding the rejection of claim 76 for indefiniteness, the Office action states at sec. 2k, "... 'each of the maps' (line 11) is indefinite because it is not made explicitly clear whether there are 2 or 3 maps that are mapped." Office action, pg. 3, sec. 2h. Applicant submits that a closer reading of claim 76 indicates that the phrase "each of the maps" includes the term "each" that singularly refers to any and all of the maps recited within independent claim 70 from which dependent claim 76 depends. The rejection of claim 76 regarding indefiniteness as to "each of the maps" is respectfully traversed.

Turning to the 35 U.S.C. § 103(a) rejections, applicant's invention relates to providing memory security (sometimes referred to as "curtained memory") and overcomes

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other memory-related problems by restricting existing code, such as drivers, without changing that code and without changing existing microprocessors. In an aspect of the invention, this may be accomplished by enabling processes to have multiple memory maps, with any given thread (unit of execution) of a process being associated with one of the maps at any given time. This may provide memory isolation without requiring a process switch. In addition to providing isolation among the various divisions of code (e.g., procedures or drivers) executed by threads within the same process, which eliminates some memory access bugs, multiple maps for a single process may be used to provide curtailed memory. To this end, memory isolation may be combined with controlled, closed memory map switching by trusted code to selectively limit the memory addresses that the threads of a process can access. For example, the threads of the process may ordinarily run at one privilege level, while map switching is only allowed at a higher privilege level. Since threads run through code, the map may be changed on entering or leaving certain verified and trusted code, thus controlling what memory addresses a thread can access based on what code is being executed at a given time. In this manner, only a small amount of trusted code decides what virtual memory a given thread can access and when, thus providing curtailed memory without changing the microprocessor design.

The present invention may be implemented with any microprocessor that has protection and a protection-context-change mechanism. For example, in an x86 processor, the protection mechanism may comprise a call gate, with map switching not allowed except at a ring 0 privilege level. To change a map for a given code module, which operates at a ring 1 or higher privilege level, a hardware call gate switches to ring 0, where it executes code that switches the map such as to access protected memory, and then calls a predefined

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service entry point (e.g., a system API) on behalf of the code module. On return from the called service, the privilege level is restored to ring 1 and the code module is returned to a different map (e.g., with less access) on exit. Note that the process (threads) request allocation of memory as before, but trusted code (e.g., as part of the operating system) is in control of which map (e.g., Map0 or Map1 in a two-map process) the thread receives. To provide a truly-safe protection mechanism, certain data structures also may need to be protected, (e.g., the tables that determine the virtual-to-physical memory address mapping need to be protected from write access by untrusted processes), otherwise an untrusted process could simply change the table data (the mappings therein) to access otherwise protected memory.

Note that the above description is for informational and example purposes only, and should not be used to interpret the claims, which are discussed below.

In contrast, Williams does not deal with changing a privilege level to a level that allows a map change responsive to a request via a process thread associated with a first memory map, performing the map change to associate a second memory map (providing different memory access with respect to the first memory map) with the process thread, and restoring the privilege level to a level that does not allow a map change. Rather, Williams is directed towards solving an entirely different problem from that solved by the present invention, essentially "to overcome the limitations of the conventional security mechanisms. It is a further object of the invention to provide a secure network in which the security mechanisms are at layer 3 of protocol hierarchy. It is another object of the invention to provide a centralized administration of a layer 3 secure network that may be distributed over the Internet. It is another object of the invention to provide a security



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device that prevents unauthorized third parties from gaining access to a host. It is another object of the invention to provide a multi-level secure network having a security device coupled between each host and the network medium." Williams, col. 4, lines 26 – 35. In other words, Williams describes a hardware network having two major components: a Network Security Center (NSC) and security network interface cards or devices. The network allows trusted users to access outside information, including the Internet, while stopping outside attackers at their point of entry. Williams, Abstract and col. 4, line 26 – col. 5, line 13. Williams further describes, "(t)he security device is a separate hardware board having a separate CPU, memory, network interface and bus architecture from the application processes on the host. A dual-ported RAM architecture guarantees that no malicious host process can tamper with the internal configuration of the security device. All network accesses must go through a security device, which implement security mechanisms for each and every access attempt. The security devices cannot be bypassed since there is no other path to or from the network." Williams, col. 5, lines 33 – 42.

Williams does not disclose, suggest, or remotely hint at responding to a request via a process thread associated with a first memory map to change a privilege level to a level that allows a map change as claimed. Nor does Williams disclose, suggest, or remotely hint at performing the map change to associate a second memory map (providing different memory access with respect to the first memory map) with the process thread and restoring the privilege level to a level that does not allow a map change also as claimed. Rather, if anything, Williams *teaches away* from doing so as Williams teaches, "(t)he network extends the mediation and cyptographic protection offered by a firewall (with its mediation and its cryptographic protection) to the network interface of each individual host

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computer." Williams, col. 5, lines 43 - 46. To that end, Williams teaches, "(t)he network provides hardware based mediation (MAC and DAC) at each host, and provides cryptographic protection (secrecy, integrity) on all host-to-host associations." Providing the mediation and cryptographic protection offered by a firewall to the network interface of each individual host computer is far different than performing the map change to associate a second memory map (providing different memory access with respect to the first memory map) with the process thread and restoring the privilege level to a level that does not allow a map change.

Similarly, Magee does not disclose or suggest: receiving a request via a process thread having a first memory map associated therewith; changing a privilege level to a level that allows a map change; performing the map change to associate a second memory map with the process thread, the second memory map providing different memory access with respect to the first memory map; and restoring the privilege level to a level that does not allow a map change. Thus, in any permissible combination, the cited references still fail to disclose or suggest applicants' invention.

By law, in order to establish prima facie obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In addition, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Further, if prior art, in any material respect teaches away from the claimed invention, the art cannot be used to support an obviousness rejection. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed Cir. 1997).

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Turning to the rejection of independent claim 1 of the present invention, claim 1 generally recites receiving a request via a process thread having a first memory map associated therewith, changing a privilege level to a level that allows a map change, performing the map change to associate a second memory map providing different memory access with respect to the first memory map with the process thread, and restoring the privilege level to a level that does not allow a map change.

The Office action cites Magee (col. 26, lines 18-26) to allege that Magee discloses "receiving a request via a process thread having a first memory map associated therewith" Office action, pg. 4, sec. 4. The Office action further cites Magee (col. 15, lines 10-34, col. 18, lines 43-44, col. 9, lines 40-56, col. 33, lines 53-61) to allege that Magee discloses "various privilege levels with maps." Office action, pg. 4, sec. 4. The Office action admits, "Magee fails to explicitly teach changing maps, performing the map change to associate a second memory map with the process thread, the second memory providing different memory access with respect to the first memory map; and restoring the privilege level to a level that does not allow a map change." Office action, pg. 4, sec. 4. Applicant submits Williams does not cure these deficiencies. The Office action cites Williams (col. 26, lines 18-26) to allege that Williams "teaches mapping and switching back and forth between separate trusted and non-trusted systems (col. 26, lines 18-26)." Office action, pg. 4, sec. 4. The cited text of Williams reads, "(t)he second host 88 has a security device 18 that permits the host 88 to operate either on the second VPN 82 or on an untrusted line 84. This ability to switch between a trusted network 82 and an untrusted network 84 is defined by the security officer at the NSC by defining multiple permitted profiles for a principal. When the principal authenticates at the security device 18 associated with this host 88, the

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principal determines which of the permitted profiles is to be used." Thus, Williams teaches that a user (security officer at the NSC) defines multiple permitted profiles for a principal and that based on the profiles the host operates on the second VPN or on an untrusted line. Williams does not perform a map change to associate a second memory map with a process thread whereby the second memory map provides different memory access with respect to a first memory map that is associated with the process thread, nor does Williams restore the privilege level to a level that does not allow a map change. In summary, the ability to switch between a trusted network and an untrusted network as defined by the security officer at the NSC by defining multiple permitted profiles for a principal is *not* receiving a request via a process thread having a first memory map associated therewith, changing a privilege level to a level that allows a map change, performing the map change to associate a second memory map that provides different memory access with respect to the first memory map with the process thread, and restoring the privilege level to a level that does not allow a map change. At least for these reasons, claim 1 and the claims that depend thereon are patentable over the cited art, whether considered alone or in any permissible combination by law.

Moreover, the Office action does not provide proper motivation for combining Magee with the subject matter discussed in Williams. However, by law, in order to support a § 103(a) rejection, there must be some teaching, suggestion, or motivation other than applicants' teachings for modifying a cited reference or combining references to achieve the claimed invention. The Office action does not indicate any suggestion or motivation in the prior art of record, either explicit or otherwise, for modifying the references or combining the references in a manner that would achieve the claimed invention, or point out any

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teaching as to how such a modification or combination might be accomplished, or what might be accomplished thereby. Instead the Office action merely recites, "It would have been obvious...to combine the feature of teach [sic] changing maps, performing the map change to associate a second memory map with the process thread, the second memory map providing different memory access with respect to the first memory map, and restoring the privilege level to a level that does not allow a map change to the existing system of Magee in order to increase the security and integrity of the system (col. 26, lines 18-26)." Office action, pgs. 4-5, sec. 4. Such broad, conclusory statements do not come close to adequately addressing the issue of motivation to combine, are not evidence of obviousness, and therefore are improper as a matter of law. In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

The Office action does not indicate any suggestion or motivation in the prior art of record, either explicit or otherwise, for combining the references in a manner that would achieve the claimed invention, and has failed to meet the requirement of establishing a case of *prima facie* obviousness. Further, any motivation for receiving a request via a process thread having a first memory map associated therewith, changing a privilege level to a level that allows a map change, performing the map change to associate a second memory map that provides different memory access with respect to the first memory map with the process thread, and restoring the privilege level to a level that does not allow a map change comes directly from applicants' teachings, not from any of the cited references. See applicants' disclosure, pg. 19, line 18 – pg. 20, line 10 and pg. 26, line 17 – pg. 28, line 4.

It is well settled that such a hindsight reconstruction based on applicants' teachings is impermissible by law. In order to support a § 103(a) rejection, there must be some

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teaching, suggestion, or motivation other than applicants' teachings for modifying a cited reference or combining references to achieve the claimed invention.

Furthermore, even if the references could be permissibly combined by law in the manner suggested by the Office action (which they are not), they would still fail to teach a method for code and thread differential addressing via multiplex page maps as recited in claim 1. At least for this additional reason, claim 1 and the claims that depend thereon are patentable over the cited references.

Similarly, independent claims 32, 64, and 70 are patentable over the cited art. Claim 32 recites: a process having at least one thread; a first memory map associated with the thread and having data therein that maps virtual memory addresses to physical memory; a second memory map having data therein that maps virtual memory addresses to physical memory, the second memory map providing different memory access with respect to the first memory map; a protection mechanism, the protection mechanism configured to allow changing of a map; and trusted code, the trusted code configured to invoke the protection mechanism to change the thread from being associated with the first map to being associated with the second map. Claim 64 recites: associating first and second address maps with a process, wherein at least the second address map includes a mapping that maps a virtual address to a physical address that is larger than the largest possible virtual memory address; receiving a request from a thread of the process to change from the first address map to the second address map; changing the first address map to the second address map; and using the mapping to access data at a physical memory location having a physical address that is larger than the largest possible virtual memory address. Claim 70 recites: associating first and second address maps with a process, wherein the second address map

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provides different memory access with respect to the first memory map; running trusted code with the first map; switching to the second map prior to running a first set of untrusted code without switching the process; and returning to the first map after completion of the untrusted code. As discussed above, the cited references, whether considered alone or in any permissible combination, do not disclose or suggest performing the map change to associate a second memory map that provides different memory access with respect to the first memory map with the process thread (e.g. the protection mechanism, the mapping, or the switching). Thus, claims 32, 64, and 70 and the claims that depend thereon are patentable over the cited references.

Turning to the rejection of dependent claims 6 and 35 of the present invention, the Office action rejected claims 6 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Magee in view of Williams, and in further view of Gulsen. Applicant respectfully submits that the rejection of claim 6 and 35 are improper. Claim 6 depends from independent claim 1. For the reasons stated above with reference to claim 1, Williams does not disclose, teach, or even suggest the limitations of claim 1. Furthermore, Williams actually *teaches away* from the limitations of claim 1, and therefore, Williams cannot be properly combined with Magee and Gulsen to reject claim 6 under 35 U.S.C. § 103(a). Claim 35 depends from independent claim 32. For the reasons stated above with reference to claim 32, Williams does not disclose, teach, or even suggest the limitations of claim 32. Furthermore, Williams actually *teaches away* from the limitations of claim 32, and therefore, Williams cannot be properly combined with Magee and Gulsen to reject claim 35 under 35 U.S.C. § 103(a).

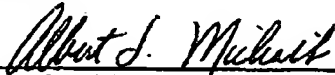
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### CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that claims 1-77 are patentable over the prior art of record. Applicants also respectfully submit that the application is in good and proper form for allowance. A favorable action on the part of the Examiner is earnestly solicited.

If in the opinion of the Examiner a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney at (425) 836-3030.

Respectfully submitted,

  
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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this Amendment, along with transmittal and facsimile cover sheet, are being transmitted by facsimile to the United States Patent and Trademark Office in accordance with 37 C.F.R. 1.6(d) on the date shown below:

Date: March 21, 2005

  
Albert S. Michalik

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